FORM PTO-1390 (REV. 1096) U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE

TRANSMITTAL LETTER TO THE UNITED STATES DESIGNATED/ELECTED OFFICE (DO/EO/US) CONCERNING A FILING UNDER 35 U.S.C. 371

ATTORNEY'S DOCKET NUMBER: S1022/8141

U S APPLICATION NO (If known, see 37 CFR 1 5): 09/367645

INTERNATIONAL APPLICATION NO.	INTERNATIONAL FILING DATE	PRIORITY DATE CLAIMED
PCT/FR98/02907	29 December 1998 (29.12.98)	30 December 1997 (30.12.97)

TITLE OF INVENTION: SUBSCRIBER INTERFACE PROTECTION CIRCUIT

APPLICANT(S) FOR DO/EO/US: BALLON, Christian

Applicant herewith submits to the United States Designated/Elected Office (DO/EO/US) the following items and other information:

1. ☒ This is a **FIRST** submission of items concerning a filing under 35 U.S.C. 371.
2. ☐ This is a **SECOND** or **SUBSEQUENT** submission of items concerning a filing under 35 U.S.C. 371.
3. ☐ This express request to begin national procedures (35 U.S.C. 371(f) at any time rather than delay examination until the expiration of the applicable time limit set in 35 U.S.C. 371(b) and PCT Articles 22 and 39(1).
4. ☒ A proper Demand for International Preliminary Examination was made by the 19th month from the earliest claimed priority date.
5. ☐ A copy of the International Application as filed (35 U.S.C. 371(c)(2)).
   a. ☐ is transmitted herewith (required only if not transmitted by the International Bureau).
   b. ☐ has been transmitted by the International Bureau.
   c. ☐ is not required, as the application was filed in the United States Receiving Office (RO/US).
6. ☒ A translation of the International Application into English (35 U.S.C. 371(c)(2)).
7. ☒ Amendments to the claims of the International Application under PCT Article 19 (35 U.S.C. 371(c)(3)).
   a. ☐ are transmitted herewith (required only if not transmitted by the International Bureau).
   b. ☐ have been transmitted by the International Bureau.
   c. ☐ have not been made; however, the time limit for making such amendments has NOT expired.
   d. ☒ have not been made and will not be made.
8. ☐ A translation of the amendments to the claims under PCT Article 19 (35 U.S.C. 371(c)(3)).
9. ☐ An oath or declaration of the inventor(s) (35 U.S.C. 371(c)(4)).
10. ☐ A translation of the annexes to the International Preliminary Examination Report under PCT Article 36 (35 U.S.C. 371(C)(5)).

Items 11. To 16. Below concern document(s) or information included:

11. ☒ An Information Disclosure Statement under 37 CFR 1.97 and 1.98.
12. ☐ An assignment document for recording. A separate cover sheet in compliance with 37 CFR 3.28 and 3.31 is included.
13. ☐ A FIRST preliminary amendment.
    ☐ A SECOND or SUBSEQUENT preliminary amendment.
14. ☐ A substitute specification.
15. ☐ A change of power of attorney and/or address letter.
16. ☐ Other items or information:

Express Mail Label No. EL 056 788 102 US
Date Mailed: August 17, 1999

(January 1997)

U.S. APPLICATION NO (If known, see 37 C F R 1 5)	INTERNATIONAL APPLICATION	ATTORNEY'S DOCKET NUMBER
09/367645	PCT/FR98/02907	S1022/8141

17. ☐ The following fees are submitted:

CALCULATIONS PTO USE ONLY

BASIC NATIONAL FEE (37 CFR 1.492(a)(1)-(5)):

Search Report has been prepared by the EPO or JPO $840.00

International preliminary examination fee paid to USPTO (37 CFR 1.482) $670.00

No international preliminary examination fee paid to USPTO (37 CFR 1.482) but international search fee paid to USPTO (37 CFR 1.445(a)(2)).. $760.00

Neither international preliminary examination fee (37 CFR 1.482) nor international search fee (37 CFR 1.445(a)(2)) paid to USPTO..... $970.00

International preliminary examination fee paid to USPTO (37 CFR 1.482) and all claims satisfied provisions of PCT Article 33(2)-(4) $96.00

ENTER APPROPRIATE BASIC FEE AMOUNT =	$ 840	
Surcharge of $130.00 for furnishing the oath or declaration later than ☐ 20 ☐ 30 months from the earliest claimed priority date (37 CFR 1.492(e)).	$	

CLAIMS	NUMBER FILED	NUMBER EXTRA	RATE		
Total Claims	- 20 =		X $18.00	$	
Independent Claims	- 3 =		X $78.00	$	
MULTIPLE DEPENDENT CLAIM(S) (if applicable)			+$260.00	$	
TOTAL OF ABOVE CALCULATIONS =				$	
Reduction by ½ for filing by small entity, if applicable. Verified Small Entity Statement must also be filed (Note 37 CFR 1.9, 1.27, 1.28).				$	
SUBTOTAL =				$	
Processing fee of $130.00 for furnishing the English translation later than ☐ 20 ☐ 30 months from the earliest claimed priority date (37 CFR 1.492(f)).				$	
TOTAL NATIONAL FEE =				$	
Fee for recording the enclosed assignment (37 CFR 1.21(h)). The assignment must be accompanied by an appropriate coversheet (37 CFR 3.28, 3.31). $40.00 per property +				$	
TOTAL FEES ENCLOSED =				$	
				Amount to be: refunded	$
				charged	$

a. ☐ A check in the amount of $ _____ To cover the above fees is enclosed.

b. ☐ Please charge my Deposit Account No. _____ In the amount of $_____ To cover the above fees. A duplicate copy of this sheet is enclosed.

c. ☐ The commissioner is hereby authorized to charge any additional fees which may be required, or credit any overpayment to Deposit Account No. 23/2825. A duplicate of this sheet is enclosed.

NOTE: Where an appropriate time limit under 37 CFR 1.494 or 1.495 has not been met, a petition to revive (37 CFR 1.137(a) or (b) must be filed and granted to restore the application to pending status.

SEND ALL CORRESPONDENCE TO

WOLF, GREENFIELD & SACKS, P.C.
600 Atlantic Avenue
Boston, Massachusetts 02210

SIGNATURE

MORRIS, James H.
NAME

34681
REGISTRATION NO

09/PRTS 09/367645
510 Rec'd PCT/PTO 14 AUG 1999

FR98/00256

SUBSCRIBER INTERFACE PROTECTION CIRCUIT

The present invention relates to circuits that protect against overvoltages, which circuits can be used in particular for subscriber line interface circuits (SLIC).

Telephone circuits connected to lines are particularly likely to be disturbed by overvoltages such as lightning discharges or accidental connections to lines of the electric power network. Further, the problem of the protection of interface circuits becomes more and more acute as these interface circuits are formed of more and more integrated circuits of smaller and smaller dimensions and accordingly, more and more sensitive to overvoltages.

The applicant has been studying SLIC protection circuits for many years and has already devised several novel circuits, monolithically implementable, which are described, in particular, in US patents N° 5274524, 5243488, 5696391 and 5684322, and in European patent applications 0742592 and 0687051.

The present invention aims at implementing a monolithic protection circuit capable of establishing a short-circuit between each conductor of a line and a ground when the voltage on this conductor exceeds a determined positive threshold or becomes smaller than a predetermined negative threshold.

The present invention also aims at implementing such a circuit which also establishes a short-circuit between a line

conductor and the ground when the current in this conductor exceeds a determined threshold.

The present invention aims at implementing such a circuit which can be manufactured by technologies compatible with that of power integrated circuits developed by the applicant.

Another object of the present invention is to provide such a circuit which is particularly reliable in operation.

Another object of the present invention is to provide such a circuit in which the on-state voltage drop is minimum (equal to the voltage drop across a thyristor only).

Another object of the present invention is to provide such a circuit which requires a very low current to be started.

To achieve these objects, the present invention provides a monolithic component that protects against line overvoltages greater than a determined positive threshold or smaller than a determined negative threshold, including in antiparallel a cathode-gate thyristor and an anode-gate thyristor connected between a first terminal of the line to be protected and a reference voltage, the gate of the cathode-gate thyristor being connected to a negative threshold voltage via a gate current amplification transistor, the gate of the anode-gate thyristor being connected to a positive threshold voltage. The monolithic component is made in a substrate of the first conductivity type divided into wells separated by isolating walls, the smaller surfaces of which are coated with insulating layers, the smaller surface of the substrate being uniformly coated with a metallization. The gate current amplification transistor of the cathode-gate thyristor is made in vertical form in a first well. The cathode-gate thyristor is implemented in vertical form in a second well. The anode-gate thyristor is implemented in vertical form in a third well. The smaller surface metallization links up the collector of the transistor, the anode of the cathode-gate thyristor, and the cathode of the anode-gate thyristor. A first front surface metallization connects the cathode of the cathode-gate thyristor to the anode of the anode-gate thyristor. A second front surface metallization connects the gate of the cathode-gate thyristor to the emitter of the

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transistor. A third front surface metallization is in contact with the gate of the anode-gate thyristor.

According to an embodiment of the present invention, the component further includes a diode, the anode of which is connected to the gate of the anode-gate thyristor. This diode is implemented in the form of a P-type region itself formed in an N-type region, the latter being formed in the cathode-gate region of the anode-gate thyristor, on the upper surface side of the component.

According to an embodiment of the present invention, the gate of the cathode-gate thyristor is connected to a second terminal of the line to be protected associated with the anode-gate thyristor, this transistor, of PNP type, being formed on the upper surface of the component, the collector region extending via isolating walls towards the smaller surface and being in contact with the smaller surface metallization.

The foregoing objects, features and advantages of the present invention, will be discussed in detail in the following non-limiting description of specific embodiments in connection with the accompanying drawings wherein:

Fig. 1A shows an example of a protection circuit;

Fig. 1B shows an embodiment according to the present invention of the circuit of Fig. 1A;

Fig. 2A shows an alternative of a protection circuit;

Fig. 2B shows an embodiment according to the present invention of the circuit of Fig. 2A;

Fig. 3A shows another alternative of a protection circuit;

Fig. 3B shows a first embodiment according to the present invention of the circuit of Fig. 3A;

Fig. 4A shows another alternative of a protection circuit; and

Fig. 4B shows a first embodiment according to the present invention of the circuit of Fig. 4A.

Fig. 1A shows a circuit that protects against overvoltages and overcurrents on a telephone line L1-L2. Each of the conductors of the telephone line includes a series resistor, respectively R1, R2,

enabling to detect overcurrents. The terminals of resistor R1 which form first input terminals of the circuit according to the present invention will be called L1A and L1B and the terminals of resistor R2 which form second input terminals of the circuit will be called L2A and L2B. Between terminal L1A and a reference potential, currently the ground, two antiparallel thyristors, that is, a cathode-gate thyristor Th1 and an anode-gate thyristor Th2, are arranged. The anode of thyristor Th1 and the cathode of thyristor Th2 are grounded, and the cathode of thyristor Th1 and the anode of thyristor Th2 are connected to terminal L1A. The gate of the cathode-gate thyristor is connected to a negative voltage source -V via an NPN-type amplifier transistor T1. The gate of the anode-gate thyristor is connected to a positive voltage source +V (in this embodiment, via a diode D1). The gates of thyristors Th1 and Th2 are connected to terminal L1B. The emitter of transistor T1 is connected to terminal L1B, its collector to the ground and its base to negative voltage -V. This assembly forms the system of protection against overvoltages and overcurrents of conductor L1. Symmetrically arranged components designated by dashed references form the protection against overvoltages and overcurrents of line L2. The operation of this circuit which will be better understood by referring to the patents and patent applications of the applicant mentioned hereabove is the following.

- If a positive overvoltage greater than voltage +V occurs on conductor L1, a current flows from the anode to the gate of anode-gate thyristor Th2 via diode D1 towards voltage +V. Thyristor Th2 turns on and shunts the overvoltage to ground.

- If a negative overvoltage smaller than voltage -V occurs on conductor L1, cathode-gate thyristor Th1 turns on and the negative overvoltage flows towards the ground. Transistor T1 increases the triggering sensitivity by acting as a gate amplifier.

- If a positive current flows through resistor R1 to generate across this resistor a voltage greater than the threshold voltage of anode-gate thyristor Th2, the latter turns on.

- If a negative current flows through resistor R1, cathode-gate thyristor Th1 turns on.

A device that protects against overvoltages and overcurrents on conductor L1 has thus effectively been obtained. The smaller portion of the circuit performs the same function for conductor L2.

It should be noted that the values of voltages +V and -V, which will for example be provided by batteries, are not necessarily equal.

The function of diodes D1 and D1' is to isolate batteries +V and -V from each other, as well as from lines L1 and L2 in the absence of overvoltages.

Fig. 1B is a simplified cross-sectional view of a semiconductive wafer incorporating the circuit of Fig. 1A. Only those elements belonging to the upper portion of the protection circuit of Fig. 1A are shown in Fig. 1B. The symmetrical components in the circuit are formed in the same way in the same silicon wafer, as will clearly appear to those skilled in the art.

The component of Fig. 1B is formed from an N-type substrate 1 divided into three wells by isolating walls 3 and 4. Each isolating wall is formed by a P-type drive-in extending from the upper and smaller surfaces of the layer, with these diffusions joining substantially at the middle of the wafer. The component is performed in a semiconductor power component technology in which a single metallization M1 covers the entire smaller surface or rear surface of the component. According to an aspect of the present invention, a technology in which the apparent portion of each isolating wall on the smaller surface side is insulated by an insulating layer is used. Reference 5 designates an insulating layer, currently silicon oxide, formed under the smaller surface of isolating wall 3 and reference 6 designates an insulating layer formed under the smaller surface of isolating wall 4.

Transistor T1 is formed in the left-hand well. This transistor is of vertical type and includes on the upper surface side a P-type base region 10 containing an N-type emitter region 11. On the smaller surface side is formed an N^+-type region 12 forming the collector contact recovered by metallization M1. It should be noted

that insulating layer 5 extends so that metallization M1 contacts N region 12 and not substrate 1 of the well. An advantage of implementing this transistor in vertical form is that it can easily withstand relatively high voltages (voltage -V is for example -50 V). Further, the connection between the collector of this transistor and the anode of cathode-gate thyristor Th1 is performed in a particularly simple and efficient way by the rear surface metallization. Further, transistor T1 has a high gain (on the order of 80 to 200) which results in a particularly low current to be supplied by battery -V upon each triggering.

Cathode-gate thyristor Th1 is formed in the central well of Fig. 1B. It is implemented in vertical form. It includes on the smaller surface side an anode region 30 and on the upper surface side a P-type region 31 and an N-type cathode region 32, currently provided with emitter short-circuits. It should be noted that insulating regions 5 and 6 extend to P region 30 so that metallization M1 does not contact the N-type central well.

In the right-hand well of Fig. 1B are formed anode-gate thyristor Th2 and diode D1. Thyristor Th2 is made in the same way as thyristor Th1 in vertical form. It includes on the smaller surface side an N cathode region 40, and on the upper surface side a deep lightly-doped P-type region 42 (made at the same time as anode region 30 of thyristor Th1) in which are formed an N-type region 43 and a P-type anode region 44. Conventionally, the anode region is provided with emitter short-circuits. Diode D1 is formed in P-type region 42 and includes in this region an N-type region 45 forming its cathode and a P-type region 46 forming its anode. This diode is a lateral diode.

On the upper surface side, the contacts are made by several metallizations:

- a metallization M2 connected to terminal L1A connecting the cathode of the cathode-gate thyristor to the anode of the anode-gate thyristor,

- a metallization M3 connected to terminal L1B connecting the gate of the cathode-gate thyristor to the emitter of transistor T1

and the gate of the anode-gate thyristor to the anode of diode D1; although, in the cross-sectional view, this metallization is shown as formed of two separate portions, it should be understood that it is one and the same metallization,

- a metallization M4 connected to terminal -V in contact with the base of transistor T1, and

- a metallization M5 connected to terminal +V in contact with the cathode of diode D1.

This structure enables to control thyristor Th1 with a very low turn-on current while this thyristor can have a high hold current (Ih). The implementation of thyristor Th2 by triple diffusion enables to obtain a sensitive thyristor.

More heavily-doped regions of same type as the underlying regions for improving the ohmicity of the contacts with the various metallizations have further been shown in the drawing. These regions are neither referenced, nor described, so as not to complicate the drawings and lengthen the description. Also, regions such as region 50 conventionally form channel stop regions to avoid the occurrence of leakage currents.

Fig. 2A shows an alternative of the circuit of Fig. 1A. Elements T1, Th1, Th2, T'1, Th'1, Th'2 reappear therein. The difference with Fig. 1A is that the gate of anode-gate thyristor Th2 is not connected to the gate of cathode-gate thyristor Th1 and is directly connected, as well as the gate of anode-gate thyristor Th'2, to positive reference voltage +V. This circuit is simpler but does not protect against positive overcurrents. It however has the advantage that the anode-gate thyristor is particularly sensitive due to the absence of anode short-circuits.

The implementation of this circuit in the form of a monolithic component appears in Fig. 2B. This drawing will not be described in detail since it is strictly similar to Fig. 1B without diode D1, that is, anode-gate region 43 of anode-gate thyristor Th2 is directly connected to positive voltage +V. It should also be noted that anode layer 44 of the anode-gate thyristor is not, in the

embodiment of Fig. 2B, provided with emitter short-circuits, which enables to obtain a more sensitive thyristor.

On the other hand, in the case of Figs. 1B and 2B, insulating layer 6 has been shown to extend to cathode contacting region 40 of anode-gate thyristor Th2. Of course, since this contact layer is of the same type as the substrate, insulating layer 6 can stop immediately beyond the smaller surface of isolating wall 4.

Fig. 3A shows another alternative of the circuit according to the present invention. This time, the structure is completely symmetrical, that is, anode-gate thyristor Th2 is, like cathode-gate thyristor Th1, associated with a gate current amplification transistor. This transistor is designated with reference T2 for thyristor Th2 and with reference T2' for thyristor Th2'. Transistors T2 and T2' are PNP transistors while transistors T1 and T'1 are NPN transistors.

An implementation according to the present invention in monolithic form of the circuit of Fig. 3A appears in a simplified cross-section in Fig. 3B. Transistor T1 and transistor Th1 are implemented in the same way as in the embodiments of Figs. 1B and 2B. Thyristor Th2 is implemented in the same way as that of Fig. 1B or of Fig. 2B according to the sensitivity desired for this thyristor. Transistor T2 is implemented between the wells containing thyristors Th1 and Th2. The collector of this transistor is formed of a P-type layer 61 deeply diffused from the upper surface. Region 61 is surrounded with a P-type drive-in 62 which joins a P-type region 63 formed from the smaller surface and on which is recovered the collector contact by metallization M1. Inside collector region 61 are formed a base region 64 and a P-type emitter region 65.

A first upper surface metallization M10 connected to terminal L1A is in contact with the cathode of thyristor Th1 and the anode of thyristor Th2 (although this metallization is shown in two portions in the drawing, it is one and the same metallization). A metallization M11 connected to terminal L1B is in contact with the gate of thyristor Th2, the emitter of transistor T2, the gate of thyristor Th1, and the emitter of transistor T1. A metallization M12

connected to terminal -V is in contact with the base of transistor T1. A metallization M13 connected to terminal +V is in contact with the base region of transistor T2.

Fig. 4A shows an alternative of the circuit of Fig. 1A. This simpler circuit does not protect against overcurrents. Elements T1, Th1, Th2, T'1, Th'1, Th'2 reappear therein. The difference with Fig. 1A is that the gates of anode-gate thyristor Th2 and cathode-gate thyristor Th1 are neither interconnected, nor connected to terminal L1B which does not exist, resistor R1 being absent.

The implementation of this circuit in the form of a monolithic component appears in Fig. 4B. This drawing will not be described in detail since it is identical to Fig. 1B except for the gate metallization: instead of having a single metallization M3, there are two separate metallizations M31 and M32 only used, respectively, to establish the connection with the emitter of transistor T1 and the connection with the anode of diode D1 (diode D1 may possibly be eliminated).

Of course, the present invention is likely to have various alterations, modifications, and improvements which will readily occur to those skilled in the art. In particular, the various described alternatives may be combined.

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CLAIMS

1. A monolithic component protecting a line against overvoltages greater than a determined positive threshold or smaller than a determined negative threshold, including in anti-parallel a cathode-gate thyristor (Th1) and an anode-gate thyristor (Th2) connected between a first terminal (L1A) of the line to be protected and a reference voltage, the gate of the cathode-gate thyristor being connected to a negative threshold voltage (-V) via a gate current amplification transistor (T1), the gate of the anode-gate thyristor being connected to a positive threshold voltage (+V), characterized in that:

- the monolithic component is made in a substrate of the first conductivity type divided into wells separated by isolating walls (3, 4), the smaller surfaces of which are coated with insulating layers (5, 6), the smaller surface of the substrate being uniformly coated with a metallization (M1),

- the gate current amplification transistor (T1) of the cathode-gate thyristor is made in vertical form in a first well,

- the cathode-gate thyristor (Th1) is implemented in vertical form in a second well,

- the anode-gate thyristor (Th2) is implemented in vertical form in a third well,

- the smaller surface metallization (M1) links up the collector of the transistor, the anode of the cathode-gate thyristor, and the cathode of the anode-gate thyristor,

- a first front surface metallization (M2) connects the cathode of the cathode-gate thyristor to the anode of the anode-gate thyristor,

- a second front surface metallization (M3) connects the gate of the cathode-gate thyristor to the emitter of the transistor, and

- a third front surface metallization is in contact with the gate of the anode-gate thyristor.

2. The component of claim 1, further including a diode (D1), the anode of which is connected to the gate of the

anode-gate thyristor, characterized in that the diode is implemented in the form of a P-type region (46) itself formed in an N-type region (45), the latter being formed in the cathode-gate region (42) of the anode-gate thyristor, on the upper surface side of the component.

3. The component of claim 1, wherein the gate of the cathode-gate thyristor is connected to a second terminal of the line to be protected (L1B).

4. The component of claim 1 or 2, further ensuring a protective function against overcurrents, in which the gates of the cathode-gate and anode-gate thyristors are interconnected and connected to a second terminal of the line to be protected (L1B).

5. The component of claim 4 taken as attached to claim 1, further including a gate current amplification transistor (T2) associated with the anode-gate thyristor, characterized in that this transistor, of PNP type, is formed on the upper surface of the component, the collector region (61) extending via isolating walls (62, 63) towards the smaller surface and being in contact with the smaller surface metallization (M1).

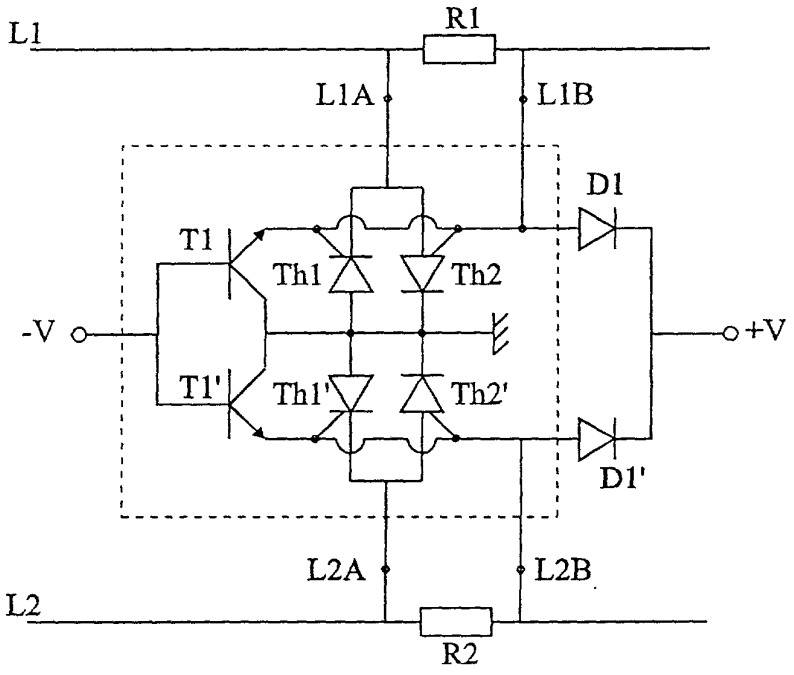
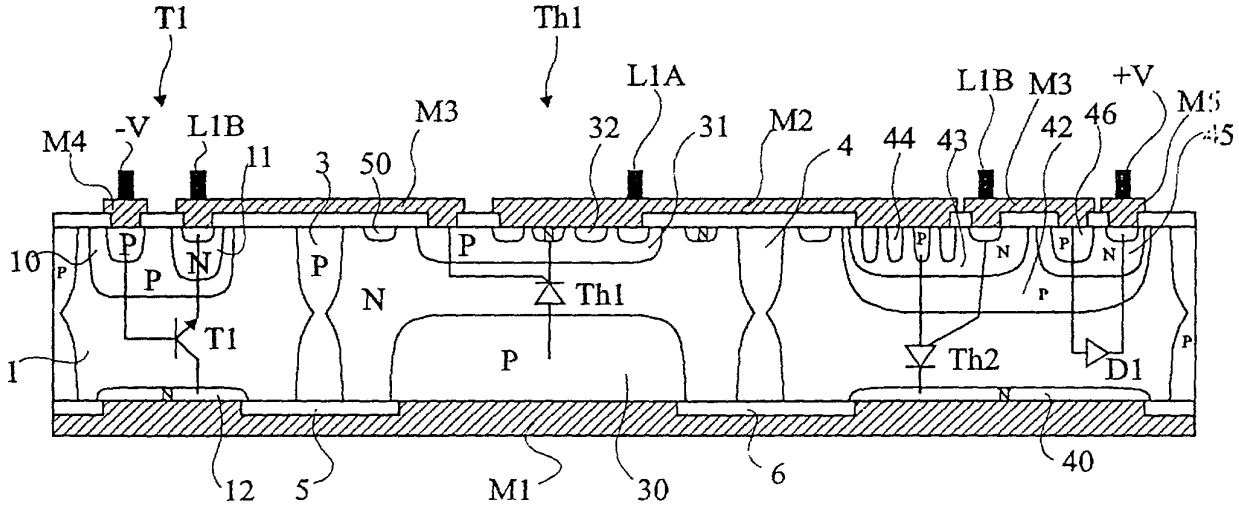

L1
R1
L1A
L1B
D1
T1
Th1
Th2
-V
+V
T1'
Th1'
Th2'
D1'
L2A
L2B
L2
R2

Fig 1A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Th1
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L1B
M3
+V
M4
-V
L1B
M3
32
31
M2
4
44
43
42
46
11
3
50
10
P
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N
Th1
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Th2
D1
12
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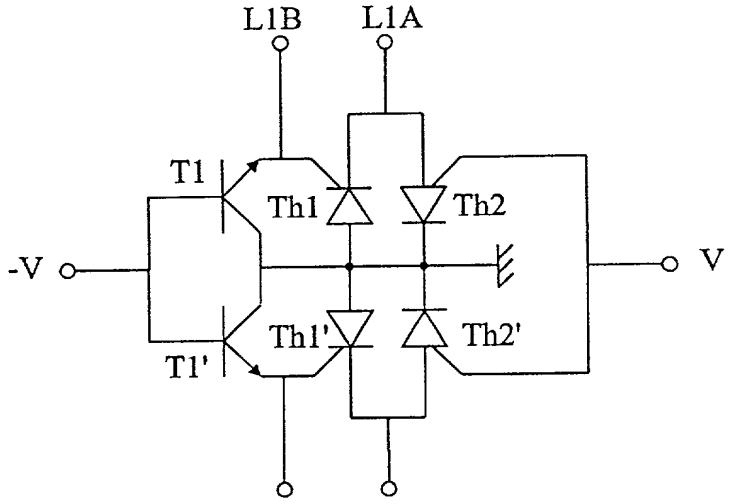
M1
30
6
40

Fig 1B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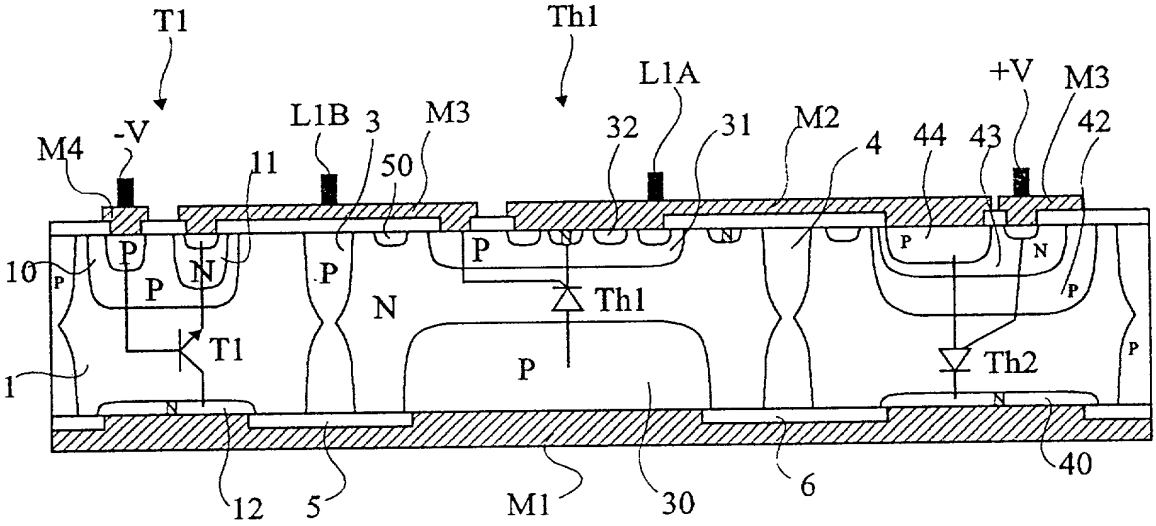
L1A
T1
Th1
Th2
-V
V
Th1'
Th2'
T1'

Fig 2A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Th1
L1A
+V
M3
L1B
3
M3
32
31
M2
44
43
42
M4
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11
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Th2
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5
M1
30
6
40

Fig 2B

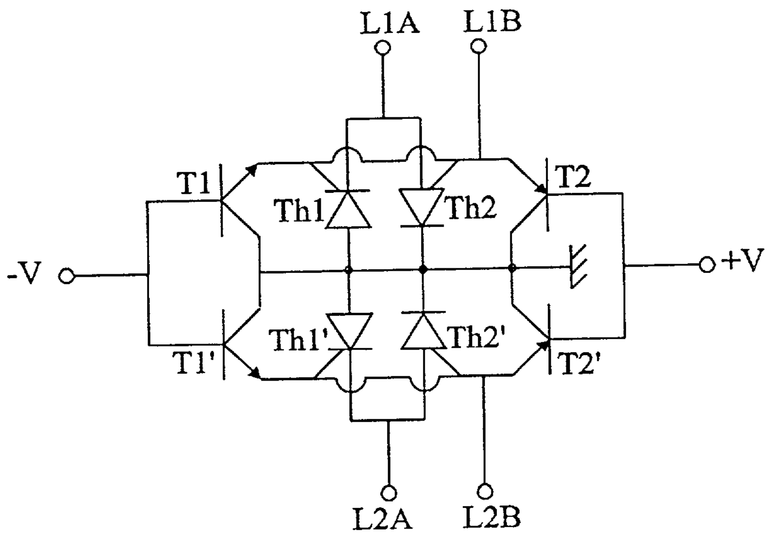

Fig 3A

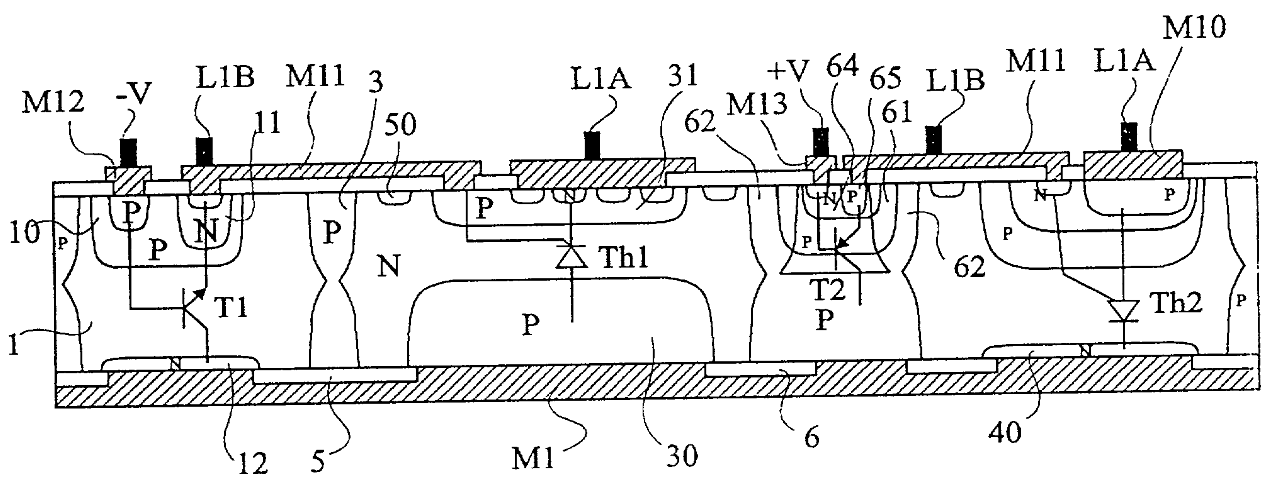

Fig 3B

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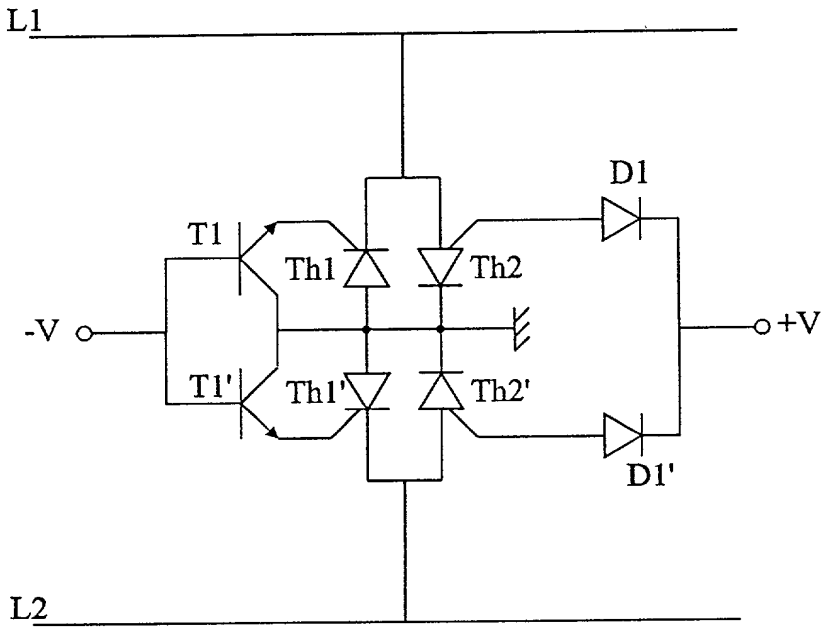

Fig 4A

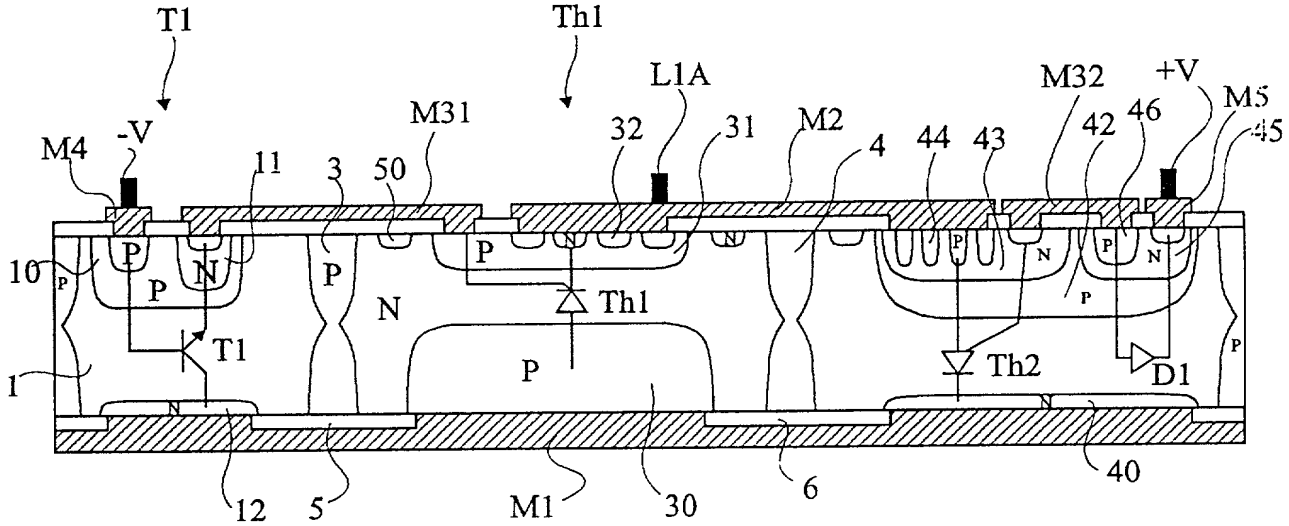

Fig 4B

Declaration and Power of Attorney for Patent Application

Déclaration et Pouvoirs pour Demande de Brevet

French Language Declaration

En tant que l'inventeur nommé ci-après, je déclare par le présent acte que:

As a below named inventor, I hereby declare that:

Mon domicile, mon adresse postale, et ma nationalité sont ceux figurant ci-dessous à côté de mon nom.

My residence, post office address and citizenship are as stated next to my name.

Je crois être le premier inventeur original et unique (si un seul nom est mentionné ci-dessous), ou l'un des premiers co-inventeurs originaux (si plusieurs noms sont mentionnés ci-dessous) de l'objet revendiqué, pour lequel une demande de brevet a été déposée concernant l'invention intitulée:

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled

SUBSCRIBER INTERFACE PROTECTION CIRCUIT

et dont la description est fournie ci-joint à moins que la case suivante n'ait été cochée:

the specification of which is attached hereto unless the following box is checked:

☒ a été déposée le 14 AOUT 1999 sous le numéro de demande des Etats-Unis ou le numéro de demande international PCT 09/367 645 et modifiée le _____ (le cas échéant).

☒ was filed on 14 AUGUST 1999 as United States Application Number or PCT International Application Number 09/367 645 and was amended on _____ (if applicable).

Je déclare par le présent acte avoir passé en revue et compris le contenu de la description ci-dessus, revendications comprises, telles que modifiées par toute modification dont il aura été fait référence ci-dessus.

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above.

Je reconnais devoir divulguer toute information pertinente à la brevetabilité, comme défini dans le Titre 37, §1.56 du Code fédéral des réglementations.

I acknowledge the duty to disclose information which is material to patentability as defined in Title 37, Code of Federal Regulations, §1.56.

French Language Declaration

Je revendique par le présent acte avoir la priorité étrangère, en vertu du Titre 35, §119(a)-(d) ou § 365(b) du Code des Etats-Unis, sur toute demande étrangère de brevet ou certificat d'inventeur ou, en vertu du Titre 35, § 365(a) du même Code, sur toute demande internationale PCT désignant au moins un pays autre que les Etats-Unis et figurant ci-dessous et, en cochant la case, j'ai aussi indiqué ci-dessous toute demande étrangère de brevet, tout certificat d'inventeur ou toute demande internationale PCT ayant une date de dépôt précédant celle de la demande à propos de laquelle une priorité est revendiquée.

I hereby claim foreign priority under Title 35, United States Code, §119(a)-(d) or § 365(b) of any foreign applications(s) for patent or inventor's certificate, or § 365(a) of any PCT International application which designated at least one country other than the United States, listed below, and have also identified below, by checking the box, any foreign application for patent or inventor's certificate, or PCT International application having a filing date before that of the application on which priority is claimed:

Prior foreign application(s)
Demande(s) de brevet antérieure(s)

(Number) (Numéro)	(Country) (Pays)	(Day/Month/Year Filed) (Jour/Mois/Année de dépôt)	Priority not claimed Droit de priorité non revendiqué
PCT/FR98/02907	PCT	29 DECEMBER 1998	☐
97716854	FRANCE	30 DECEMBER 1997	☐

Je revendique par le présent acte tout bénéfice, en vertu du Titre 35 §119(e) du Code des Etats-Unis, de toute demande de brevet provisoire effectuée aux Etats-Unis et figurant ci-dessous.

I hereby claim the benefit under Title 35, United States Code, § 119(e) of any United States provisional application(s) listed below.

(Application No.) (N° de demande)	(Filing Date) (Date de dépôt)

Je revendique par le présent acte, le bénéfice, en vertu du Titre 35 § 120 du Code des Etats-Unis, de toute demande de brevet effectuée aux Etats-Unis, ou en vertu du Titre 35, § 365(c) du même Code, de toute demande internationale PCT désignant les Etats-Unis et figurant ci-dessous et, dans la mesure où l'objet de chacune des revendications de cette demande de brevet n'est pas divulgué dans la demande antérieure américaine ou internationale PCT, en vertu des dispositions du premier paragraphe du Titre 35, § 112 du Code des Etats-Unis, je reconnais devoir divulguer toute information pertinente à la brevetabilité, comme défini dans le Titre 37, § 1.56 du Code Fédéral des réglementations, dont j'ai pu disposer entre la date de dépôt de la demande antérieure et la date de dépôt de la demande nationale ou internationale PCT de la présente demande:

I hereby claim the benefit under Title 35, United States Code, §120 of any United States application(s) or § 365(c) of any PCT international application(s) designating the United States, listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States or PCT International application in the manner provided by the first paragraph of Title 35, United States Code, §112, I acknowledge the duty to disclose information which is material to patentability as defined in Title 37, Code of Federal Regulations, §1.56 which became available between the filing date of the prior application and the national or PCT International filing date of this application:

(Application No.) (N° de Demande)	(Filing Date) (Date de Dépôt)	(Status)(Patented, pending abandoned) (Statut)(breveté, en cours d'examen, abandonné)

Je déclare par le présent acte que toute déclaration ci-incluse est, à ma connaissance, véridique et que toute déclaration formulée à partir de renseignements ou de suppositions est tenue pour véridique; et de plus, que toutes ces déclarations ont été formulées en sachant que toute fausse déclaration volontaire ou son équivalent est passible d'une amende ou d'une incarcération, ou des deux, en vertu de la Section 1001 du Titre 18 du Code des Etats-Unis, et que de telles déclarations volontairement fausses risquent de compromettre la validité de la demande de brevet ou du brevet délivré à partir de celle-ci.

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

French Language Declaration

POUVOIR: En tant que l'inventeur cité, je désigne par la présente l'(les) avocat(s) et/ou agent(s) suivant(s) pour qu''il(s) poursuive(nt) la procédure de cette demande de brevet et traite(nt) toute affaire s'y rapportant avec l'Office des brevets et des marques: *(mentionner le nom et le numéro d'enregistrement).*

POWER OF ATTORNEY: As a named inventor, I hereby appoint the following attorney(s) and/or agent(s) to prosecute this application and transact all business in the Patent and Trademark Office connected therewith. *(list name and registration number)*

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(Supply similar information and signature for third and sub-sequent joint inventors.)